

SSSSSSSSSSSSS	YYY	YYY	SSSSSSSSSSSSS	LLL	0000000000	AAAAAAA
SSSSSSSSSSSSS	YYY	YYY	SSSSSSSSSSSSS	LLL	0000000000	AAAAAAA
SSSSSSSSSSSSS	YYY	YYY	SSSSSSSSSSSSS	LLL	0000000000	AAAAAAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSSSSSSSSS	YYY	YYY	SSSSSSSSSS	LLL	000	000 AAA AAA
SSSSSSSSSS	YYY	YYY	SSSSSSSSSS	LLL	000	000 AAA AAA
SSSSSSSSSS	YYY	YYY	SSSSSSSSSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAAA AAAAAA
SSS	YYY	YYY	SSS	LLL	000	000 AAAA AAAAAA
SSS	YYY	YYY	SSS	LLL	000	000 AAAA AAAAAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSS	YYY	YYY	SSS	LLL	000	000 AAA AAA
SSSSSSSSSS	YYY	SSSSSSSSSS	LLLLLLLLLLLL	0000000000	AAA	AAA
SSSSSSSSSS	YYY	SSSSSSSSSS	LLLLLLLLLLLL	0000000000	AAA	AAA
SSSSSSSSSS	YYY	SSSSSSSSSS	LLLLLLLLLLLL	0000000000	AAA	AAA

_S2
Syn

SS1
SS1
SS1
SS1
SS1
SS1
SS1
SYS
SYS
SYS
TRY
UNL
WR1

AAAAAA	DDDDDDDD	PPPPPPPP	SSSSSSSS	UU	UU	BBBBBBBB	77777777	999999	000000
AAAAAA	DDDDDDDD	PPPPPPPP	SSSSSSSS	UU	UU	BB	77777777	999999	000000
AA	AA	DD	DD	PP	PP	BB	77	99	00
AA	AA	DD	DD	PP	PP	BB	77	99	00
AA	AA	DD	DD	PP	PP	BB	77	99	00
AA	AA	DD	DD	PP	PP	BB	77	99	00
AA	AA	DD	DD	PPPPPPPP	SSSSSS	UU	UU	99999999	00000000
AA	AA	DD	DD	PPPPPPPP	SSSSSS	UU	UU	99999999	00000000
AAAAAAA	DD	DD	PP	SS	UU	BB	77	99	00
AAAAAAA	DD	DD	PP	SS	UU	BB	77	99	00
AA	AA	DD	DD	PP	SS	UU	BB	99	00
AA	AA	DD	DD	PP	SS	UU	BB	99	00
AA	AA	DDDDDDDD	PP	SSSSSSSS	UUUUUUUUUU	BBBBBBBB	77	999999	000000
AA	AA	DDDDDDDD	PP	SSSSSSSS	UUUUUUUUUU	BBBBBBBB	77	999999	000000

LL	IIIIII	SSSSSSSS
LL	IIIIII	SSSSSSSS
LL	IIII	SS
LLLLLLLL	IIII	SSSSSSSS
LLLLLLLL	IIII	SSSSSSSS

(3)	148	CISINT - CI INTERRUPT HANDLER
(4)	237	DRSINT - DR INTERRUPT HANDLER
(5)	537	UBA\$INITIAL - CPU-DEPENDENT UNIBUS ADAPTER INITIALIZATION
(5)	418	MASSBUS ADAPTER INTERRUPT DISPATCHER
(5)	535	MASSPUS ADAPTER INITIALIZATION
(6)	567	INI\$MPMADP - BUILD ADP AND INITIALIZE MULTI-PORT MEMORY
(6)	661	MA\$INITIAL - INITIALIZE MULTI-PORT MEMORY ADAPTER
(6)	730	INTER-PROCESSOR REQUEST HANDLER
(6)	847	REPORT RESOURCE AVAILABILITY TO INTERESTED PORTS

```
0000 1 .NOSHOW CONDITIONALS
0000 2
0000 3
0000 4
0000 5
0000 6
0000 7
0000 8
0000 9
0000 10
0000 11
0000 12
0000 13 .TITLE ADPSUB790 - ADAPTER SUBROUTINES FOR VAX 11/790
0000 14
0000 15
0000 16
0000 17
0000 18
0000 19
0000 20
0000 21
0000 22 .IDENT 'V04-000'
0000 23
0000 24 :***** *
0000 25 :* 26 :* COPYRIGHT (c) 1978, 1980, 1982, 1984 BY
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0000 42 :* SOFTWARE ON EQUIPMENT WHICH IS NOT SUPPLIED BY DIGITAL.
0000 43 :*
0000 44 :*
0000 45 :***** *
0000 46 :
0000 47 : Facility: System bootstrapping and initialization
0000 48 :
0000 49 : Abstract: This module contains initialization routines that are loaded
0000 50 : during system initialization (rather than linked into the system).
0000 51 :
0000 52 : Environment: Mode = KERNEL, Executing on INTERRUPT stack, IPL=31
0000 53 :
0000 54 : Author: Kerbey T. Altmann           Creation date: 30-Oct-1982
0000 55 :
0000 56 : Modification history:
0000 57 :
0000 58 : V03-007 TCM0002      Trudy C. Matthews   04-Jun-1984
0000 59 :           Include more 780-specific code for the 11/790 version of
0000 60 :           this routine.
0000 61 :
0000 62 : V03-006 KPL0001      Peter Lieberwirth   12-Apr-1984
0000 63 :           Init ADPSL_SHB properly again; V03-004 ASSUMED this field
0000 64 :           was at a certain constant offset, and a change to the ADP
0000 65 :           moved it. Note - this is a 780 change only.
0000 66 :
0000 67 : V03-005 KDM0081      Kathleen D. Morse   13-Sep-1983
0000 68 :           Create version for Micro-VAX I.
0000 69 :
0000 70 : V03-004 ROW0196      Ralph O. Weber     27-JUL-1983
0000 71 :           Correct INISMPMADP so the ADPSL_SHB is correctly initialized
```

0000 72 : to zero.
0000 73 :
0000 74 : V03-003 MSH0001 Maryann Hinden 06-Dec-1982
0000 75 : Add initialization for DW750.
0000 76 :
0000 77 : V03-002 ROW0142 Ralph O. Weber 23-NOV-1982
0000 78 : Correct JMP in multiport memory interrupt dispatching code
0000 79 : prototype, MPMINTD, to a JSB. MASINT expects to receive
0000 80 : control via a JSB.
0000 81 :
0000 82 : V03-001 TCM0001 Trudy C. Matthews 8-Nov-1982
0000 83 : Initialize field ADP\$L_AVECTOR in INISMPMADP.
0000 84 :
0000 85 :--

00000001	0000	90	
	0000	92	C780_LIKE = 1
	0000	94	
	0000	98	
	0000	102	
	0000	106	
	0000	107	: MACRO LIBRARY CALLS
	0000	108	:
	0000	109	\$ADPDEF
	0000	110	\$CRBDEF
	0000	111	\$DCDEF
	0000	112	\$DDBDEF
	0000	113	\$DDTDEF
	0000	114	\$DYNDEF
	0000	115	\$IDBDEF
	0000	116	\$MBADEF
	0000	117	\$MCHKDEF
	0000	118	\$MPMDEF
	0000	119	\$NDTDEF
	0000	120	\$PRDEF
	0000	121	\$PTEDEF
	0000	122	\$RPBDEF
	0000	123	\$SSSDEF
	0000	124	\$UBADEF
	0000	125	\$UBIDEF
	0000	126	
	0000	127	\$UCBDEF
	0000	128	\$VADEF
	0000	129	\$VECDEF
	0000	130	
	0000	132	\$CEBDEF
	0000	133	\$FKBDEF
	0000	134	\$IPLDEF
	0000	135	\$PRIDEF
	0000	136	\$PRQDEF
	0000	137	\$RSNDEF
	0000	138	\$SHBDEF
	0000	139	\$SHDDEF
	0000	141	
	0000	145	
00000000	146		.PSECT SYSLOA,LONG

; Define ADP offsets.
 ; Define CRB offsets.
 ; Define AT codes.
 ; Define DDB offsets.
 ; Define DDT offsets.
 ; Define data structure type codes.
 ; Define interrupt dispatcher offsets.
 ; Define MASSBUS registers.
 ; Define machine check masks.
 ; Define multi-port memory.
 ; Define nexus device types.
 ; Define IPR numbers.
 ; Define Page Table Entry bits.
 ; Define Restart Parameter Block fields.
 ; Define system service codes.
 ; Define UBA register offsets.
 ; Define UNIBUS interconnect
 ; register offsets.
 ; Define unit control block.
 ; Define virtual address fields.
 ; Define vec offsets.

; COMMON EVENT BLOCK
 ; FORK BLOCK
 ; INTERRUPT PRIORITY LEVELS
 ; PRIORITY INCREMENT DEFINITIONS
 ; INTER-PROCESSOR REQUEST
 ; RESOURCE NUMBER DEFINITIONS
 ; SHARED MEMORY CONTROL BLOCK
 ; SHARED MEMORY DATAPAGE

```

0000 148 .SBTTL CISINT - CI INTERRUPT HANDLER
0000 149 :+
0000 150 : CISINT - CI INTERRUPT HANDLER
0000 151 :
0000 152 : THIS MODULE IS A DUMMY CI32 INTERRUPT HANDLER WHICH IS USED
0000 153 : UNTIL THE REAL CI DRIVER (PADRIVER) IS LOADED. IT ALSO CONTAINS
0000 154 : A DUMMY CI32 CONTROLLER INITIALIZATION ENTRY POINT.
0000 155 :
0000 156 : INPUTS:
0000 157 :
0000 158 : THE STACK ON ENTRY IS AS FOLLOWS:
0000 159 :
0000 160 : 0(SP) ADDRESS OF IDB ADDRESS
0000 161 : 4(SP) - 16(SP) SAVED R2 - R5
0000 162 : 20(SP) INTERRUPT PC
0000 163 : 24(SP) INTERRUPT PSL
0000 164 :
0000 165 : OUTPUTS:
0000 166 :
0000 167 : NONE
0000 168 :
0000 169 : SIDE EFFECTS:
0000 170 :
0000 171 : INTERRUPTS ARE DISABLED ON THE CI32
0000 172 :
0000 173 :
0000 174 :
0000 175 :
0000 176 :
0000 177 : SPAREGDEF -- Define offsets to CI registers and fields in the registers.
0000 178 :
0000 179 :
0000 180 :
0000 181 SDEFINI PAREG
0000 182 :
0000 183 SDEF PA_CNF .BLKL 1 ; Configuration register
0004 184 :
0004 185 VIELD PA_CNF,0,<-
0004 186 <ADPTYP,,M>,- ; Define config register fields:
0004 187 <PFD,,M>,- ; Adapter type code
0004 188 <TDEAD,,M>,- ; Powerfail disable
0004 189 <TFAIL,,M>,- ; Transmit dead
0004 190 <,5>,- ; Transmit fail
0004 191 <CRD,,M>,- ; 5 unused bits
0004 192 <RDS,,M>,- ; CRD on port init'd read
0004 193 <CXTER,,M>,- ; RDS on port init'd read
0004 194 <RDTO,,M>,- ; SBI error confirm
0004 195 <CSTMO,,M>,- ; Port init'd read timeout on SBI
0004 196 <,1>,- ; Port init'd command xmit timeout
0004 197 <PUP,,M>,- ; 1 unused bit
0004 198 <PDN,,M>,- ; Adapter power up
0004 199 > ; Adaptor power down
0004 200 :
0004 201 SDEF PA_PMC .BLKL 1 ; Port maint control/status register
0008 202 :
0008 203 VIELD PA_PMC,0,<-
0008 204 <MIN,,M>,- ; Define register fields:
0008 205 <MTD,,M>,- ; Maint initialized
0008 206 <MIE,,M>,- ; Maint timer disable
0008 207 > ; Maint interrupt enable

```

	0008	207	<MIF,,M>,-	: Maint interrupt flag
	0008	208	>	:
	0008	209		
	0008	210	\$DEFEND PAREG	
	0000	211		
	0000	212	CISINT::	
64	53 9E	DO 0000	213 MOVL a(SP)+,R3	: GET ADDRESS OF IDB
64	54 63	DO 0003	214 MOVL IDBSL(CSR(R3),R4)	: GET ADDRESS OF FIRST CSR
	00400000 8F	DO 0006	215 MOVL #PA_CNF_M_PUP,PA_CNF(R4)	: CLEAR POWER UP
	00800000 8F	DO 000D	216 MOVL #PA_CNF_M_PDN,PA_CNF(R4)	: CLEAR POWER DOWN
	04 A4 01	DO 0014	217 MOVL #PA_PMC_M_MIN,PA_PMC(R4)	: SET MAINTENCE INITIALIZE
	52 8E	7D 0018	218 MOVQ (SP)+,R2	: RESTORE REGISTERS
	54 8E	7D 001B	219 MOVQ (SP)+,R4	
		02 001E	REI	
		001F	221	
		001F	224	
		001F	225 CISINITIAL::	: CONTROLLER INITIALIZATION
		001F	226 CISSHUTDOWN::	: CONTROLLER SHUTDOWN
		001F	227	
04 A4 01	DO 001F	230		
	0023	231	MOVL #PA_PMC_M_MIN,PA_PMC(R4)	: SET MAINTENCE INITIALIZE
	05 0023	234		
		235 RSB		

0024 237 .SBTTL DRSINT - DR INTERRUPT HANDLER
0024 238 :+
0024 239 : DRSINT - DR INTERRUPT HANDLER
0024 240 :
0024 241 : THIS MODULE IS A DUMMY DR32 INTERRUPT HANDLER WHICH IS USED
0024 242 : UNTIL THE REAL DR DRIVER (XFDRIVER) IS LOADED. IT ALSO CONTAINS
0024 243 : A DUMMY DR32 CONTROLLER INITIALIZATION ENTRY POINT.
0024 244 :
0024 245 : INPUTS:
0024 246 :
0024 247 : THE STACK ON ENTRY IS AS FOLLOWS:
0024 248 :
0024 249 : 0(SP) ADDRESS OF IDB ADDRESS
0024 250 : 4(SP) - 16(SP) SAVED R2 - R5
0024 251 : 20(SP) INTERRUPT PC
0024 252 : 24(SP) INTERRUPT PSL
0024 253 :
0024 254 : OUTPUTS:
0024 255 :
0024 256 : NONE
0024 257 :
0024 258 : SIDE EFFECTS:
0024 259 :
0024 260 : INTERRUPTS ARE DISABLED ON THE DR32
0024 261 :-
0024 262 :
0024 263 :
0024 264 :
0024 265 :
0024 266 : DR32 DCR REGISTER DEFINITIONS
0024 267 :
0024 268 :-
0024 269 :
0024 270 : \$DEFINI DR
0000 271 SDEF DR_DCR .BLKL 1 : DR32 CONTROL REGISTER
0004 272 _VIELD DR_DCR,0,<-
0004 273 <ADPTYP,8>,- : ADAPTER TYPE
0004 274 <ID2ERR,M>,- : ID2 ERROR
0004 275 <ID2TOS,2>,- : ID2 TIME-OUT STATUS
0004 276 <,1>,- : RESERVED
0004 277 <ID1ERR,M>,- : ID1 ERROR
0004 278 <ID1TOS,2>,- : ID1 TIME-OUT STATUS
0004 279 <RDS,,M>,- : READ DATA SUBSTITUTE
0004 280 <CRD,,M>,- : CORRECTED READ DATA
0004 281 <DCRHLT,,M>,- : DCR HALT
0004 282 <DCRABT,,M>,- : DCR ABORT INTERRUPT
0004 283 <PKTINT,,M>,- : PACKET INTERRUPT
0004 284 <INTENB,,M>,- : INTERRUPT ENABLE
0004 285 <,1>,- : RESERVED
0004 286 <PWR_UP,,M>,- : ADAPTER POWER UP
0004 287 <PWR_DN,,M>,- : ADAPTER POWER DOWN
0004 288 <EXTABT,,M>,- : EXTERNAL ABORT
0004 289 <,1>,- : RESERVED
0004 290 <IMPDEP,6>,- : IMPLEMENTATION DEPENDENT BITS
0004 291 >
0004 292 :
0004 293 : DCR CONTROL FIELD A CODES (USED WHEN WRITING TO DCR)
0004 294 :
00000100 0004 295 UCR_K_CLR_PWR_UP=*X100

00000200	0004	296	DCR_K_CLR_PWRDN = "X200	: CLEAR POWER DOWN
00000300	0004	297	DCR_K_CLR_EXTABT = "X300	: CLEAR EXTERNAL ABORT
00000400	0004	298	DCR_K_CLR_ABTINT = "X400	: CLEAR ABORT INTERRUPT
00000500	0004	299	DCR_K_CLR_INTENB = "X500	: CLEAR INTERRUPT ENABLE
00000600	0004	300	DCR_K_SET_INTENB = "X600	: SET INTERRUPT ENABLE
00000700	0004	301	DCR_K_CLR_HLT = "X700	: CLEAR HALT
		302		
		303	: DCR CONTROL FIELD B CODES (USED WHEN WRITING TO DCR)	
		304		
00001000	0004	305	DCR_K_CLR_CRD = "X1000	: CLEAR CRD
00002000	0004	306	DCR_K_SET_TEXTABT = "X2000	: SET EXTERNAL ABORT
00003000	0004	307	DCR_K_CLR_PKTINT = "X3000	: CLEAR PACKET INTERRUPT
00004000	0004	308	DCR_K_RESET = "X4000	: RESET
00005000	0004	309	DCR_K_SET_OSEQ_TST = "X5000	: SET OSEQ TEST
00006000	0004	310	DCR_K_CLR_OSEQ_TST = "X6000	: CLEAR OSEQ TEST
		311	SDEFEND DR	
		312		
		313	DRSINT::	
64 00000100	53 8F	D0 0024	MOVL a(SP)+, R3	: GET ADDRESS OF IDB
64 00000200	54 63	D0 0027	MOVL IDBSL CSR(R3), R4	: GET ADDRESS OF FIRST CSR
	002A		MOVL #DCR_K_CLR_PWRUP, DR_DCR(R4)	: CLEAR POWER UP
	0031		MOVL #DCR_K_CLR_PWRDN, DR_DCR(R4)	: CLEAR POWER DOWN
	52 8E	7D 0038	MOVQ (SP)‡, R2	: RESTORE REGISTERS
	54 BE	7D 003B	MOVQ (SP)+, R4	
		02 003E	REI	
		003F		
		003F		
		003F	DRSINITIAL::	: CONTROLLER INITIALIZATION
		003F	DRSSHUTDOWN::	: CONTROLLER SHUTDOWN
		003F		
64 4000 8F	3C	003F	325	
		0044	326	
	05	0044	327	
		330	MOVZWL #DCR_K_RESET, (R4)	: RESET DR (R4 POINTS TO CSR)
		331		
		334	RSB	
		335		

0045 337 .SBTTL UBASINITIAL - [CPU-DEPENDENT UNIBUS ADAPTER INITIALIZATION
 0045 338 :+
 0045 339 : UBASINITIAL - UNIBUS ADAPTER INITIALIZATION
 0045 340 :
 0045 341 : THIS ROUTINE IS CALLED VIA A JSB INSTRUCTION AT SYSTEM STARTUP AND AFTER
 0045 342 : A POWER RECOVERY RESTART TO ALLOW INITIALIZATION OF UNIBUS ADAPTERS.
 0045 343 : (POWERFAIL AND INITADP)
 0045 344 :
 0045 345 : INPUTS:
 0045 346 :
 0045 347 : R2 = ADDRESS OF ADAPTER CONTROL BLOCK (11/780 AND 11/750)
 0045 348 : R4 = ADDRESS OF UNIBUS ADAPTER CONFIGURATION STATUS REGISTER (11/780)
 0045 349 :
 0045 350 : ALL INTERRUPTS ARE LOCKED OUT.
 0045 351 :
 0045 352 : OUTPUTS:
 0045 353 :
 0045 354 : THE UNIBUS ADAPTER IS INITIALIZED AND INTERRUPTS ARE ENABLED.
 0045 355 :-
 0045 356 :
 0045 357 UBASINITIAL:: :UNIBUS ADAPTER INITIALIZATION
 0045 358 :
 0045 359 :
 0045 360 :
 08 64 00 D2 0045 361 MCOML #0,UBASL_CSR(R4) :CLEAR ALL ADAPTER CONFIGURATION ERRORS
 08 A4 00 D2 0048 362 MCOML #0,UBASL_SR(R4) :CLEAR ALL ADAPTER STATUS BITS
 50 0256 C2 3C 004C 363 MOVZWL ADPSW_UMR_DIS(R2),R0 :PICK UP THE NUMBER OF UMR'S TO DISABLE
 50 50 16 78 0051 364 ASHL #UBASV_CR_MRDSB-4,R0,R0 :DIVIDE BY 16 THEN SHIFT INTO POSITION
 C9 0055 365 BISL3 #UBASM_CR_SUEFIE!- :ENABLE INTERRUPTS
 0056 366 UBASM_CR_BRIE!-
 0056 367 UBASM_CR_CNFIE!-
 0056 368 UBASM_CR_USEFIE!-
 0056 369 UBASM_CR_IFSIE,-
 0056 370 R0,UBASL_C(R(R4))
 005E 371 :
 005E 372 :
 005E 373 :
 005E 374 :
 005E 375 :
 005E 376 :
 005E 377 :
 005E 378 :
 005E 379 :
 005E 380 :
 005E 381 :
 005E 382 :
 005E 383 : NO SPECIAL INIT FOR 11/730 OR UVAX I
 05 005E 384 10\$: :;
 005E 385 RSB :
 005F 386 :
 005F 387 : IGNORE UNEXPECTED UNIBUS INTERRUPTS
 005F 388 :
 005F 389 :
 005F 390 : ALIGN LONG
 0060 391 :
 0060 392 UBASINTO:: : PASSIVE RELEASES THROUGH VECTOR 0
 0060 393 :
 0060 394 INCL #IOSGL_UBA_INTO : COUNT THEM
 0060 395 BRB UBA_UNEXINT : JOIN COMMON CODE, VECTORS ARE ALIGNED
 0068 396 :
 0068 397 :
 0068 398 :
 0068 399 :
 0068 400 : NOTE: UBASUNEXINT is the label in the EXEC that is a JMP #UBA_UNEXINT.
 0068 401 : This seeming duplicity is necessary since there is code that must
 0068 402 : refer to the EXEC address from within the SYSLOA image.
 0068 403 :
 0068 404 UBA_UNEXINT:: : UNEXPECTED INTERRUPT CODE

		0068	405		
		0068	407		
		0068	408		
3F	BA	0068	409	POPR	#^H<R0,R1,R2,R3,R4,R5>
		006A	412		
02		006A	414	REI	

: FOR 780-LIKE PROCESSORS, RESTORE
SAVED REGISTERS
: FOR 11/750, NO REGISTERS SAVED
: IGNORE INTERRUPT

006B 418 .SBTTL MASSBUS ADAPTER INTERRUPT DISPATCHER
 006B 419 :+
 006B 420 : MBASINT - MASSBUS ADAPTER INTERRUPT DISPATCHER
 006B 421 :
 006B 422 : THIS ROUTINE IS ENTERED VIA A JSB INSTRUCTION WHEN AN INTERRUPT OCCURS
 006B 423 : ON A MASSBUS ADAPTER. THE STATE OF THE STACK ON ENTRY IS:
 006B 424 :
 006B 425 : 00(SP) = ADDRESS OF IDB ADDRESS.
 006B 426 : 04(SP) = SAVED R2.
 006B 427 : 08(SP) = SAVED R3.
 006B 428 : 12(SP) = SAVED R4.
 006B 429 : 16(SP) = SAVED R5.
 006B 430 : 20(SP) = INTERRUPT PC.
 006B 431 : 24(SP) = INTERRUPT PSL.
 006B 432 :
 006B 433 : INTERRUPT DISPATCHING OCCURS AS FOLLOWS:
 006B 434 :
 006B 435 : IF THE INTERRUPTING ADAPTER IS CURRENTLY OWNED AND THE OWNER UNIT
 006B 436 : IS EXPECTING AN INTERRUPT, THEN THAT UNIT IS DISPATCHED FIRST. ALL
 006B 437 : OTHER UNITS ARE DISPATCHED BY READING THE ATTENTION SUMMARY REG-
 006B 438 : ISTER AND SCANNING FOR UNITS THAT HAVE ATTENTION SET. AS EACH UNIT
 006B 439 : IS FOUND, ITS ATTENTION SUMMARY BIT IS CLEARED AND THEN A TEST IS
 006B 440 : MADE TO DETERMINE IF AN INTERRUPT IS EXPECTED ON THE UNIT. IF YES,
 006B 441 : THEN THE DRIVER IS CALLED AT ITS INTERRUPT RETURN ADDRESS. ELSE
 006B 442 : THE DRIVER IS CALLED AT ITS UNSOLICITED INTERRUPT ADDRESS. AS EACH
 006B 443 : CALL TO THE DRIVER RETURNS, THE ATTENTION SUMMARY REGISTER IS RE-
 006B 444 : READ AND AN ATTEMPT IS MADE TO FIND ANOTHER UNIT TO DISPATCH. WHEN
 006B 445 : NO UNITS REQUESTING ATTENTION REMAIN, THE INTERRUPT IS DISMISSED.
 006B 446 :-

006B 447 :
 006B 448 :.ALIGN LONG
 006C 449 :
 53 00 BE DD 006C 450 MBASINT::
 54 63 DD 0070 451 MOVL a(SP),R3 ;MASSBUS ADAPTER INTERRUPT DISPATCHER
 00800000 8F D3 0073 452 MOVL IDBSL_CSR(R3),R4 ;GET ADDRESS OF IDB
 64 61 12 007A 453 0073 ;GET ADDRESS OF CONFIGURATION STATUS REGISTE
 007C 454 ;
 007C 455 0073 ;
 007C 456 0073 ;
 007C 457 0079 ;
 007C 458 007A ;
 007C 459 007C ;
 007C 460 007C ;
 007C 461 007C ;
 007C 462 007C ;
 007C 463 007C ;
 007C 464 007C ;
 007C 465 007C ;
 007C 466 007C ;
 007C 467 007C ;
 007C 468 007C ;
 007C 469 0080 ;
 21 64 A5 01 0082 470 0080 ;
 52 0090 C5 9A 0082 471 0080 ;
 53 00 BE DD 008C 472 10\$:
 08 A4 00 D2 0093 473 0080 ;
 52 0410 C4 DD 0097 474 0080 ;
 52 0B 00 EA 009C 475 0080 ;
 0A 12 00A1 476 0080 ;
 5E 04 C0 00A3 477 0080 ;
 52 8E 7D 00A6 478 0080 ;
 54 8E 7D 00A9 479 0080 ;
 02 00AC 480 0080 ;
 00AD 481 0080 ;
 00AD 482 0080 ;
 006C 470 0080 ;
 006C 471 0080 ;
 006C 472 0080 ;
 006C 473 0080 ;
 006C 474 0080 ;
 006C 475 0080 ;
 006C 476 0080 ;
 006C 477 0080 ;
 006C 478 0080 ;
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 006C 496 0080 ;
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55	18 A342	DO 00AD	483	20\$: MOVL UCBLST(R3)[R2],RS	:GET ADDRESS OF UCB OR INTERRUPT DISPATCHER
	22 55	E8 00B2	484	BLBS R5,40\$:IF LBS INTERRUPT DISPATCHER FOR MULTI-
		00B5	485		: DEVICE CONTROLLER
0410	C4 01	52 78 0085	486	ASHL R2,#1,MBASL_AS(R4)	:CLEAR ATTENTION SUMMARY BIT
		55 D5 0088	487	TSTL R5	:SEE IF UCB DEFINED
		CD 13 008D	488	BEQL 10\$:IF EQL NONE DEFINED
09 64	A5 01	F5 008F	489	#UCBSV INT_UCBSW_STS(R5)	:30\$: IF CLR, INTERRUPT NOT EXPECTED
53	10 A5	7D 00C4	490	MOVA UCBSL_FR3(R5),R3	:RESTORE DRIVER CONTEXT
	OC BS	16 00C8	491	JSB UCBSL_FPC(R5)	:CALL DRIVER AT INTERRUPT RETURN ADDRESS
	BF	11 00CB	492	BRB 10\$:
53	0088 C5	DO 00CD	493		
04	B3 16	00D2	494	30\$: MOVL UCBSL_DDT(R5),R3	:GET ADDRESS OF DDT
B5	11 00D5	00D7	495	JSB ADDT\$C_UNSOLINT(R3)	:CALL UNSOLICITED INTERRUPT ROUTINE
		00D7	496	BRB 10\$:
7E	DC 00D7	00D7	497		
75	16 00D9	00D9	498	40\$: MOVPSL -(SP)	:READ CURRENT PSL
AF	11 00DB	00DB	499	JSB -(R5)	:CALL SLAVE CONTROLLER INTERRUPT DISPATCHER
		00DD	500	BRB 10\$:
		00DD	501		
		00DD	503		
		00DD	504		
		00DD	505	: IN CASE OF ADAPTER POWER DOWN BIT ASSERTED, RETRIEVE ADP ADDRESS AND JUMP	
		00DD	506	: TO ADAPTER ERROR ROUTINE IN SYSLOA780.	
		00DD	507	:	
		00DD	508		
54	14 A3 FF1C	DO 00DD	509	45\$: MOVL UCBLST(R3),R4	:GET ADP ADDRESS
	31 00E1	00E1	510	BRW EXESRA780_INT	:JUMP TO ERROR ROUTINE
	00E4	00E4	511		
	00E4	533			

1 3

00E4 535 .SBTTL MASSBUS ADAPTER INITIALIZATION
00E4 536 ::+
00E4 537 :: MBASINITIAL - MASSBUS ADAPTER INITIALIZATION
00E4 538 ::
00E4 539 :: THIS ROUTINE IS CALLED VIA A JSB INSTRUCTION AT SYSTEM STARTUP AND AFTER
00E4 540 :: A POWER RECOVERY RESTART TO ALLOW INITIALIZATION OF MASSBUS ADAPTERS.
00E4 541 ::
00E4 542 :: INPUTS:
00E4 543 ::
00E4 544 :: R4 = CSR ADDRESS OF MASSBUS ADAPTER.
00E4 545 :: R5 = ADDRESS OF ADAPTER IDB.
00E4 546 ::
00E4 547 :: ALL INTERRUPTS ARE LOCKED OUT.
00E4 548 ::
00E4 549 :: OUTPUTS:
00E4 550 ::
00E4 551 :: THE MASSBUS ADAPTER IS INITIALIZED AND INTERRUPTS ARE ENABLED.
00E4 552 ::-
00E4 553 ::
00E4 554 MBASINITIAL:: :MASSBUS ADAPTER INITIALIZATION
00E4 555 ::
01 DO 00E4 558 MOVL #MBASM_CR_INIT,- :INITIALIZE MASSBUS ADAPTER
04 A4 00E6 559 MBASL_CTR4)
04 DO 00E8 560 MOVL #MBASM_CR_IE,- :ENABLE INTERRUPTS
04 A4 00EA 561 MBASL_CTR4)
00EC 564
05 00EC 565 RSB

00ED 567 .SBTTL INISMPMADP - BUILD ADP AND INITIALIZE MULTI-PORT MEMORY
00ED 568 ::+
00ED 569 :: INISMPMADP IS CALLED AFTER MAPPING THE REGISTERS FOR A MULTI-PORT
00ED 570 :: MEMORY ADAPTER. AN ADAPTER CONTROL BLOCK IS ALLOCATED AND FILLED.
00ED 571 :: THE HARDWARE ADAPTER IS THEN INITIALIZED BY CALLING MPMSINITIAL.
00ED 572 ::
00ED 573 :: NOTE: THIS ROUTINE HAS BEEN LOCATED HERE IN SYSLOAXXX.EXE INSTEAD OF
00ED 574 :: INILOA.EXE BECAUSE IT CAN BE CALLED WHILE THE SYSTEM IS RUNNING
00ED 575 :: LONG AFTER INILOA.EXE HAS BEEN DELETED!!!
00ED 576 ::
00ED 577 :: INPUT:
00ED 578 :: R4 - nexus identification number of this nexus
00ED 579 ::
00ED 580 :: OUTPUTS:
00ED 581 :: ALL REGISTERS PRESERVED
00ED 582 :-
00000010 00ED 583
00ED 584 NUMMPMVEC = 16 ; NUMBER OF INTER-PORT INTERRUPT VECTORS
00ED 585
00ED 586 INISMPMADP:: ; INITIALIZE MPM DATA STRUCTURES
00ED 587
05 00ED 588 RSB ; DUMMY ENTRY FOR SYSGEN
00EE 589
00EE 590

00EE 661 .SBTTL MASINITIAL - INITIALIZE MULTI-PORT MEMORY ADAPTER
00EE 662 :++
00EE 663 :
00EE 664 : MPPSINITIAL - INITIALIZE MULTI-PORT MEMORY ADAPTER
00EE 665 :
00EE 666 : THIS ROUTINE IS CALLED AT SYSTEM INITIALIZATION AND AFTER A POWER
00EE 667 : RECOVERY RESTART TO INITIALIZE THE PORT ADAPTER BY CLEARING ANY
00EE 668 : ERRORS AND ENABLING ALL INTERRUPTS.
00EE 669 :
00EE 670 : INPUTS:
00EE 671 :
00EE 672 : R4 = ADDR OF ADAPTER CSR.
00EE 673 :
00EE 674 : IPL = 31
00EE 675 :
00EE 676 : OUPUTS:
00EE 677 :
00EE 678 : ANY ERRORS IN PORT ARE CLEARED AND ALL INTERRUPTS ARE ENABLED.
00EE 679 :--
00EE 680 :
00EE 681 MASINITIAL:: ; INITIALIZE PORT
00EE 682 :
05 00EE 684 RSB
00EF 685

00EF 730 .SBTTL INTER-PROCESSOR REQUEST HANDLER
00EF 731 :++
00EF 732 :
00EF 733 : FUNCTIONAL DESCRIPTION:
00EF 734 :
00EF 735 : THIS ROUTINE IS CALLED BY A DRIVER OR AN EXEC FUNCTION TO
00EF 736 : EITHER SEND A REQUEST TO OR JUST INTERRUPT ANOTHER PROCESSOR
00EF 737 : THAT IS CONNECTED TO A PORT OF THE MULTIPOINT MEMORY.
00EF 738 :
00EF 739 : INPUTS:
00EF 740 :
00EF 741 : R4 = ADAPTER CONTROL BLOCK ADDRESS.
00EF 742 : R5 = IF LSS 0 - ADDRESS OF A FORK BLOCK TO USE IF REQUEST
00EF 743 : BLOCK IS NOT AVAILABLE.
00EF 744 : IF GEQ 0 - PORT NUMBER OF PROCESSOR TO JUST INTERRUPT.
00EF 745 :
00EF 746 : OUTPUTS:
00EF 747 :
00EF 748 : WHEN THIS ROUTINE IS CALLED WITH A FORK BLOCK ADDRESS, IT WILL
00EF 749 : ATTEMPT TO ALLOCATE A REQUEST BLOCK. IF THE REQUEST FAILS,
00EF 750 : THE CONTEXT OF THE CALLER WILL BE SAVED IN THE FORK BLOCK, THE
00EF 751 : FORK BLOCK WILL BE INSERTED IN THE REQUEST BLOCK WAIT
00EF 752 : QUEUE AND A RETURN TO THE CALLER'S CALLER IS EXECUTED.
00EF 753 :
00EF 754 : IF A REQUEST BLOCK IS ALLOCATED SUCCESSFULLY, CONTROL WILL
00EF 755 : RETURN TO THE CALLER VIA A CO-ROUTINE CALL SO THE CALLER CAN
00EF 756 : FILL-IN THE REQUEST BLOCK.
00EF 757 :
00EF 758 : THE CALLER WILL THEN PERFORM ANOTHER CO-ROUTINE CALL TO RETURN
00EF 759 : TO THIS ROUTINE SO THE BLOCK CAN BE INSERTED IN THE DESIRED
00EF 760 : PROCESSOR'S INTER-PROCESSOR REQUEST QUEUE. IF IT IS THE
00EF 761 : FIRST REQUEST IN THE QUEUE AN INTER-PORT INTERRUPT WILL
00EF 762 : ALSO BE REQUESTED TO WAKE-UP THE DISPATCHER ON THE PORT.
00EF 763 :
00EF 764 :
00EF 765 : IF THIS ROUTINE IS CALLED WITH A PORT NUMBER INSTEAD OF A
00EF 766 : FORK BLOCK ADDRESS, IT WILL JUST REQUEST AN INTERRUPT FOR
00EF 767 : THE PROCESSOR ON THE SPECIFIED PORT. IT IS THEN UP TO THE
00EF 768 : INTERRUPTED PROCESSOR TO DETERMINE WHAT THE INTERRUPT WAS
00EF 769 : FOR.
00EF 770 :
00EF 771 : R0 = SUCCESS OR FAILURE OF OPERATION. THIS SHOULD BE CHECKED
00EF 772 : BY THE CALLER BOTH TIMES THIS ROUTINE RETURNS.
00EF 773 :
00EF 774 : R3,R4,R5 ARE PRESERVED.
00EF 775 :
00EF 776 :--
00EF 777 :
00EF 778 : MASREQUEST:: : REQUEST HANDLER
00EF 779 :
00FO 781 : RSB
00FO 782 :

00F0 847 .SBTTL REPORT RESOURCE AVAILABILITY TO INTERESTED PORTS
00F0 848 ;++
00F0 849 ;
00F0 850 ; FUNCTIONAL DESCRIPTION:
00F0 851 ;
00F0 852 ; THIS ROUTINE IS CALLED TO REPORT TO ANY PROCESSORS THAT A RESOURCE
00F0 853 ; HAS BEEN MADE AVAILABLE.
00F0 854 ;
00F0 855 ; INPUTS:
00F0 856 ;
00F0 857 ; R0 = RESOURCE NUMBER OF RESOURCE MADE AVAILABLE.
00F0 858 ; R1 = SHARED MEMORY CONTROL BLOCK (SHB) ADDRESS.
00F0 859 ;
00F0 860 ; OUTPUTS:
00F0 861 ;
00F0 862 ; ANY PROCESSORS WAITING FOR THE SPECIFIED RESOURCE ARE INTERRUPTED
00F0 863 ; TO NOTIFY THEM THE RESOURCE IS AVAILABLE.
00F0 864 ;
00F0 865 ; R0,R1,R2,R3 ARE NOT PRESERVED.
00F0 866 ;--
00F0 867 ;
00F0 868 MASRAVAIL::
00F0 869 ;
05 00F0 871 RSB
00F1 872 ;
00F1 1175 .END

ADPSW_UMR_DIS
 C780_CIKE
 CISINITIAL
 CISINT
 CISSHUTDOWN
 CPU_TYPE
 DCR_K_CLRPWRDN
 DCR_K_CLRPWRUP
 DCR_K_RESET
 DDTSL_UNSOLINT
 DR\$INIT
 DR\$SHUTDOWN
 DR_DCR
 EXESRH780_INT
 IDBSL_ADP
 IDBSL_CSR
 IDBSL_OWNER
 IDBSL_UCBLST
 INISMMPMDP
 IOSGL_UBA_INTO
 MASINITIAL
 MASRAVAIL
 MASREQUEST
 MBASINITIAL
 MBASINT
 MBASL_AS
 MBASL_CR
 MBASL_CSR
 MBASL_SR
 MBASM_CR_IE
 MBASM_CR_INIT
 MBASM_CSR_PD
 NUMMPPVEC
 PA_CNF
 PA_CNF_M_PDN
 PA_CNF_M_PUP
 PA_PMC
 PA_PMC_M_MIN
 PRS_SID_TYP730
 PRS_SID_TYP750
 PRS_SID_TYP780
 PRS_SID_TYP790
 PRS_SID_TYPUV1
 SIZ...
 UBASINITIAL
 UBASINTO
 UBASL_CR
 UBASL_CSR
 UBASL_SR
 UBASM_CR_BRIE
 UBASM_CR_CNFIE
 UBASM_CR_IFSIE
 UBASM_CR_SUEFIE
 UBASM_CR_USEFIE
 UBASV_CR_MRDSB
 UBA_UNEXINT

= 00000256	UCBSB_SLAVE	= 00000090
= 00000001	UCBSL_DDT	= 00000088
0000001F RG 02	UCBSL_FPC	= 0000000C
00000000 RG 02	UCBSL_FR3	= 00000010
0000001F RG 02	UCBSV_INT	= 00000001
= 00000004	UCBSW_STS	= 00000064
= 00000200		
= 0000100		
= 00004000		
= 00000004		
0000003F RG 02		
00000024 RG 02		
0000003F RG 02		
00000000		
***** X 02		
= 00000014		
= 00000000		
= 00000004		
= 00000018		
000000ED RG 02		
***** X 02		
000000EE RG 02		
000000F0 RG 02		
000000EF RG 02		
000000E4 RG 02		
0000006C RG 02		
= 0000410		
= 00000004		
= 00000000		
= 00000008		
= 00000004		
= 00000001		
= 00800000		
= 00000010		
00000000		
= 00800000		
= 00400000		
00000004		
= 00000001		
= 00000003		
= 00000002		
= 00000001		
= 00000004		
= 00000007		
= 00000006		
00000045 RG 02		
00000060 RG 02		
= 00000004		
= 00000000		
= 00000008		
= 00000020		
= 00000004		
= 00000040		
= 00000008		
= 00000010		
= 0000001A		
00000068 RG 02		

```
+-----+
! Psect synopsis !
+-----+
```

PSECT name

	Allocation	PSECT No.	Attributes																
ABS	00000000 (0.)	00 (0.)	NOPIC	USR	CON	ABS	LCL	NOSHR	NOEXE	NORD	NOWRT	NOVEC	BYTE						
\$ABSS	00000008 (8.)	01 (1.)	NOPIC	USR	CON	ABS	LCL	NOSHR	EXE	RD	WRT	NOVEC	BYTE						
SYSLOA	000000F1 (241.)	02 (2.)	NOPIC	USR	CON	REL	LCL	NOSHR	EXE	RD	WRT	NOVEC	LONG						

```
+-----+
! Performance indicators !
+-----+
```

Phase

Phase	Page faults	CPU Time	Elapsed Time
Initialization	29	00:00:00.05	00:00:02.13
Command processing	129	00:00:00.57	00:00:03.97
Pass 1	541	00:00:13.90	00:00:53.79
Symbol table sort	0	00:00:02.21	00:00:07.70
Pass 2	113	00:00:02.88	00:00:10.56
Symbol table output	8	00:00:00.08	00:00:00.29
Psect synopsis output	2	00:00:00.01	00:00:00.53
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	624	00:00:19.70	00:01:18.97

The working set limit was 1950 pages.

131956 bytes (258 pages) of virtual memory were used to buffer the intermediate code.

There were 110 pages of symbol table space allocated to hold 2138 non-local and 6 local symbols.

1179 source lines were read in Pass 1, producing 13 object records in Pass 2.

38 pages of virtual memory were used to define 37 macros.

```
+-----+
! Macro library statistics !
+-----+
```

Macro library name

Macro library name	Macros defined
\$255\$DUA28:[SYSLOA.OBJ]790DEF.MLB;1	0
\$255\$DUA28:[SYS.OBJ]LIB.MLB;1	25
\$255\$DUA28:[SYSLIB]STARLET.MLB;2	7
TOTALS (all libraries)	32

2215 GETS were required to define 32 macros.

There were no errors, warnings or information messages.

MACRO/LIS=LI\$:ADPSUB790/OBJ=OBJ\$:ADPSUB790 MSRC\$:CPUSW790/UPDATE=(ENH\$:CPUSW790)+MSRC\$:ADPSUB/UPDATE=(ENH\$:ADPSUB)+EXECMLS/LIB+LIB\$

0392 AH-BT13A-SE
VAX/VMS V4.0

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LIS

CLUSTRL0A
LIS

CONMAN
LIS

ADPSUB290
LIS

CLUMESSAC
LIS